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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,715	02/06/2002	Ryo Tatsumi	36856.607	4041

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EXAMINER	
LE, DUY K	

ART UNIT	PAPER NUMBER
2685	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,715	TATSUMI ET AL.	
	Examiner	Art Unit	
	Duy K Le	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8, 10, 12, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Hasegawa et al. (U.S. Patent 4,651,344).

As to claim 1, Figure 2 in Hasegawa shows a mixer comprising:

a balun (10) including two balanced lines each having a first end that is short-circuited and a second end that defines a balanced terminal, and an unbalanced line having a first end that is free and a second end that defines an unbalanced terminal (see Col. 3, lines 32-59);

a pair of mixer diodes (17, 18) connected to respective ones of the balanced terminals (see Col. 3, lines 32-59);

an LO port (3) connected to the unbalanced terminal (see Col. 3, lines 32-59);

a high-pass filter (20) (see Col. 3, lines 32-59);

an RF port (1) connected to a node between said mixer diodes through said high-pass filter (see Col. 3, lines 32-59);

a low-pass filter (20) (see Col. 3, lines 32-59); and

an IF port (2) connected to the node between said mixer diodes through said low-pass filter (see Col. 3, lines 32-59);

wherein said balun, said pair of mixer diodes, said high-pass filter, and said low-pass filter are integrated into a multilayer substrate that includes a plurality of sheet layers stacked on each other (see Col. 3, lines 32-59, Col. 4, lines 48-57, Col. 5, lines 44-64, and Figures 4A, 4B, 5A to 5C); and

the multilayer substrate has first external terminals that respectively define said LO port, said RF port, and said IF port at the side surfaces thereof, and has second external terminals that define a ground, at least one of the second external terminals being arranged between two of the first external terminals (see Col. 3, lines 32-59, Col. 4, lines 48-57, Col. 5, lines 44-64, and Figures 4A, 4B, 5A to 5C).

As to claim 2, the Hasegawa reference discloses a mixer according to claim 1, wherein each of the balanced lines and the unbalanced line includes strip line electrodes, and is arranged in the lower section of the multilayer substrate with respect to the stacking direction of the multilayer substrate (see Col. 3, lines 32-59, Col. 4, lines 48-57, Col. 5, lines 44-64, and Figures 4A, 4B, 5A to 5C).

As to claim 3, the Hasegawa reference discloses a mixer according to claim 2, wherein at least one of said high-pass filter and said low-pass filter includes at least one capacitor, each capacitor including at least one capacitor electrode, and is located in the upper section of the multilayer substrate with respect to the stacking direction thereof, a ground electrode being provided between said at least one capacitor electrode and the strip line electrodes (see Col. 3, lines 32-59, Col. 4, lines 48-57, Col. 5, lines 44-64, and Figures 2, 4A, 4B, 5A to 5C).

As to claim 4, the Hasegawa reference discloses a mixer according to claim 1, wherein the mixer is a single balanced mixer (see Col. 1, lines 55-63).

As to claim 5, the Hasegawa reference discloses a mixer according to claim 1, wherein the high-pass filter blocks LO and IF signals and passes only an RF signal (see Col. 3, lines 54-59).

As to claim 6, the Hasegawa reference discloses a mixer according to claim 1, wherein the low-pass filter blocks LO and RF signals and passes only an IF signal (see Col. 3, lines 54-59).

As to claim 7, the Hasegawa reference discloses a mixer according to claim 1, wherein the high-pass filter (20) includes an inductor and at least two capacitors (see Figure 2 and Col. 3, lines 54-67. The strip lines connected to ground are functionally equivalent to inductors).

As to claim 8, the Hasegawa reference discloses a mixer according to claim 1, wherein the low-pass filter (19) includes at least two inductors and a capacitor (see Figure 2 and Col. 3, lines 54-67. The strip line connecting RF terminal 1 to connecting portion 24 are functionally equivalent to two inductors: one inductor between the two capacitors and one inductor from second capacitor to connecting portion 24).

As to claim 10, the Hasegawa reference discloses a mixer according to claim 1, wherein the multilayer substrate includes strip line electrodes which define the balanced lines and the unbalanced line of the balun, strip line electrodes, capacitor electrodes, and ground electrodes which define the high-pass filter, and a capacitor electrode and ground electrodes which define the low-pass filter (see Col. 3, lines 32-59, Col. 4, lines 48-57, Col. 5, lines 44-64, and Figures 2, 4A, 4B, 5A to 5C).

As to claim 12, the Hasegawa reference discloses a mixer according to claim 1, wherein the low-pass filter is located in the upper section of the multilayer substrate (see Col. 3, lines 32-59, Col. 4, lines 48-57, Col. 5, lines 44-64, and Figures 2, 4A, 4B, 5A to 5C).

As to claim 13, the Hasegawa reference discloses a mixer according to claim 1, wherein the balanced and unbalanced lines of the balun include a ground electrode, a capacitor and strip line electrodes, wherein the ground electrode is provided between the capacitor and the strip line electrodes (see Col. 3, lines 32-59, Col. 4, lines 48-57, Col. 5, lines 44-64, and Figures 2, 4A, 4B, 5A to 5C).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,651,344 to Hasegawa et al. in view of Trinh (U.S. Patent 5,265,266).

As to claim 9, the Hasegawa reference discloses a mixer according to claim 1. However, it does not expressly disclose the sheet layers of the multilayer substrate are made of ceramic material. The Trinh reference teaches the sheet layers of the multilayer substrate are made of ceramic material (see Col. 6, lines 7-11).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the mixer of Hasegawa wherein the sheet layers of the

multilayer substrate are made of ceramic material, as taught by Trinh, in order to manufacture a circuit substrate.

As to claim 11, the Hasegawa reference discloses a mixer according to claim 1, wherein the external terminals are arranged to extend from the side surfaces to the bottom surface of the multilayer substrate, the balanced and the unbalanced lines that constitute the balun are provided in the lower section of the multilayer substrate with respect to the stacking direction. However, it does not expressly disclose the multilayer substrate is made of ceramic material. The Trinh reference teaches the multilayer substrate is made of ceramic material (see Col. 6, lines 7-11).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the mixer of Hasegawa wherein the multilayer substrate is made of ceramic material, as taught by Trinh, in order to manufacture a circuit substrate.

5. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,651,344 to Hasegawa et al. in view of Lee et al. (U.S. Patent 6,483,355).

As to claims 14-17, the Hasegawa reference discloses a converter comprising: a mixer according to claims 1-4 (see Col. 1, lines 6-8). However, it does not disclose a converter further comprising an RF amplifying unit connected to said RF port of said mixer; a PLL oscillation unit connected to said LO port of said mixer; and an intermediate frequency amplifying unit connected to said IF port of said mixer.

The Lee reference teaches a converter further comprising an RF amplifying unit connected to said RF port of said mixer; a PLL oscillation unit connected to said LO port of said mixer; and an intermediate frequency amplifying unit connected to said IF port of said mixer (see Figure 1 and Col. 1, line 44 to Col. 2, line 13).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the converter of Hasegawa to further comprise an RF amplifying unit connected to said RF port of said mixer; a PLL oscillation unit connected to said LO port of said mixer; and an intermediate frequency amplifying unit connected to said IF port of said mixer, as taught by Lee, in order to demodulate an input RF signal.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Onishi et al. (U.S. Patent 4,340,975) discloses microwave mixing circuit and a VHF-UHF tuner having the mixing circuit.

b. Takahashi et al. (U.S. Patent 4,864,644) discloses VHF-UHF mixer having a balun.

c. Carter (U.S. Patent 5,266,963) discloses integrated antenna/mixer for the microwave and millimetric wavebands.

d. Yanagimoto (U.S. Patent 5,465,416) discloses balanced output high-frequency transducers and mixers using the same with symmetrically located components.

e. Li et al. (U.S. Patent 5,774,801) discloses high dynamic range mixer having low conversion loss, low local oscillator input power, and high dynamic range and a method for designing the same.

f. Nakajima et al. (U.S. Patent 6,456,836) discloses frequency multiplier and wireless device incorporating same.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duy K Le whose telephone number is 703-305-5660. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F Urban can be reached on 703-305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Duy Le
June 24, 2004

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